

FIG 1

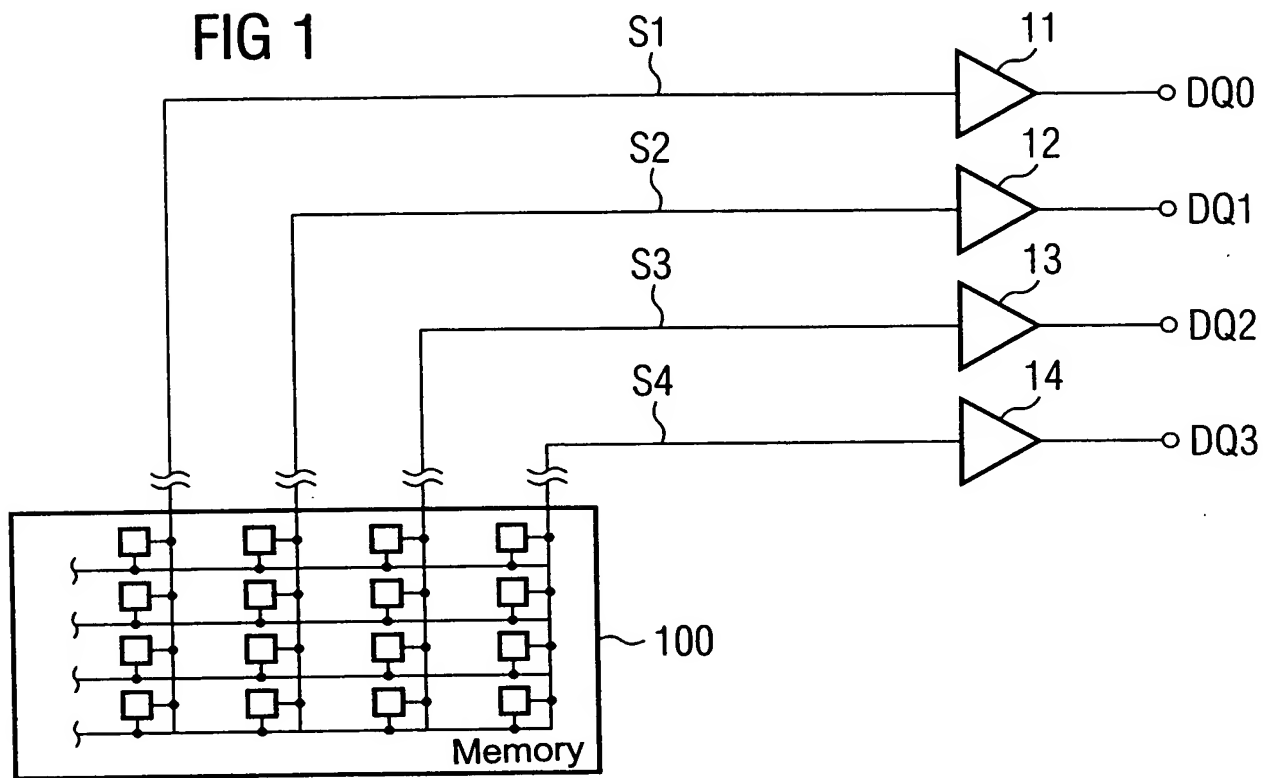


FIG 4

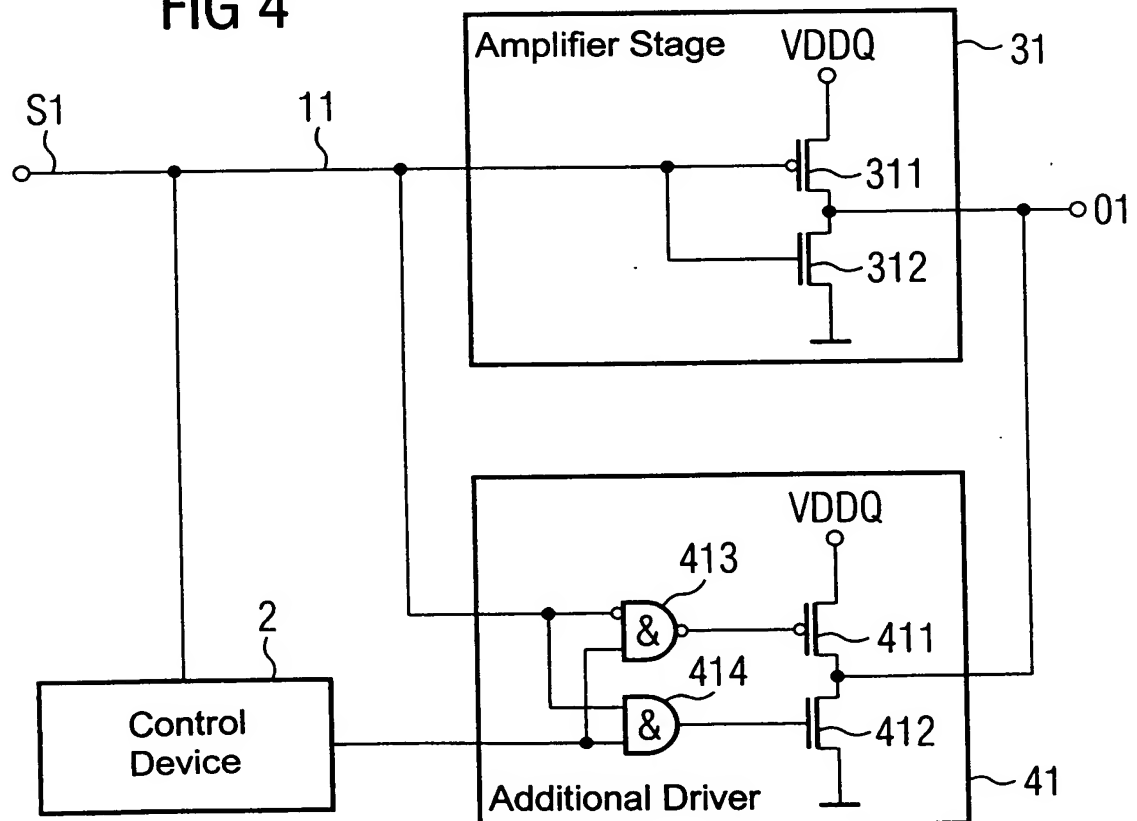


FIG 2

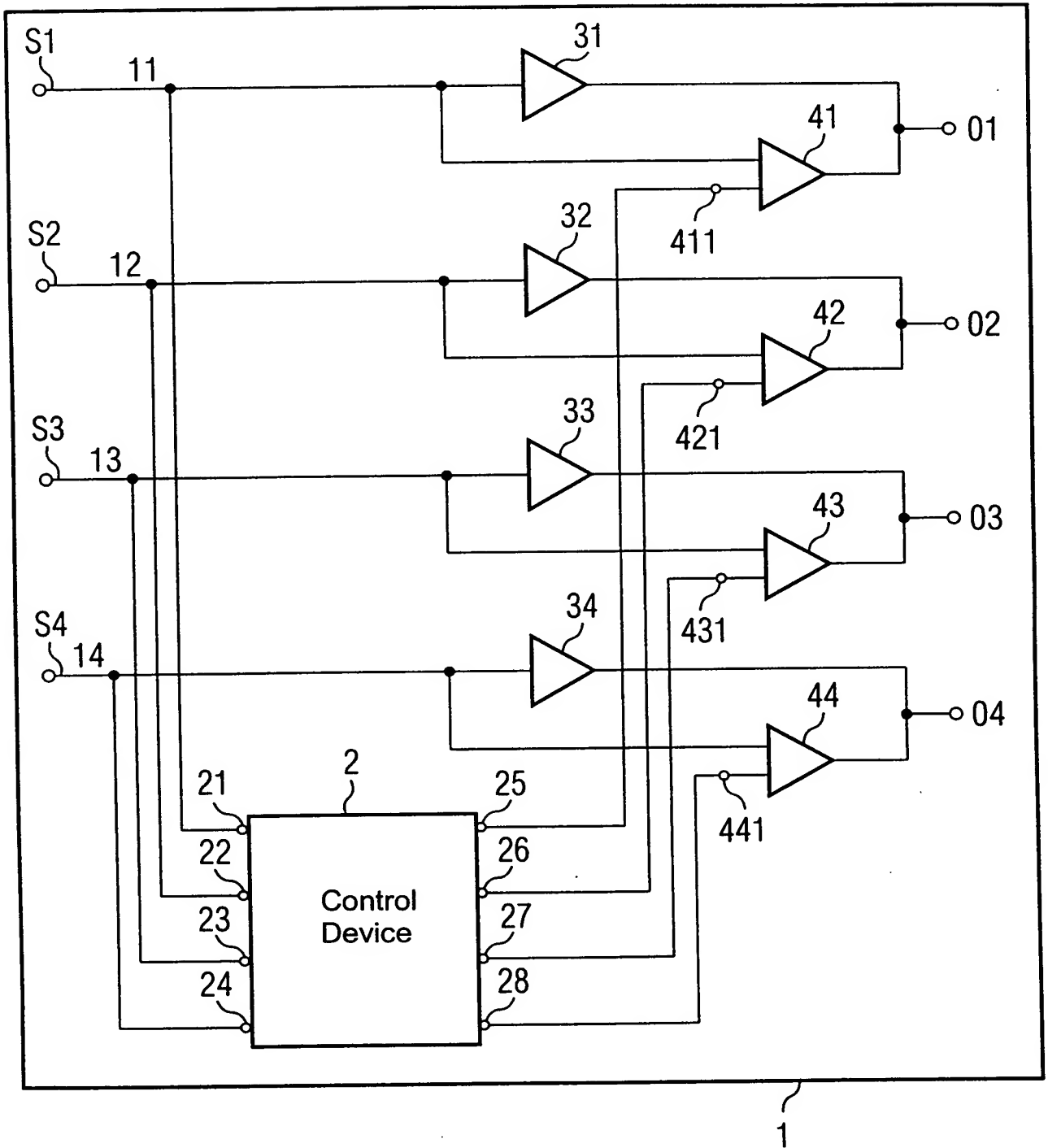


FIG 3

301		303		305		307		309		311	
302		304		306		308		310		311	
SL	DW1	DW2	DW3	SZP1	SZP2	SZW1	SZW2	Control Signals Generated After Transfer DW1 DW2		Driver Stages Transfer DW1 to DW3	Additional Driver Stages Transfer DW2 DW3
S1	0	0	1	00	01	0	1	-	1	31=en	41=dis 41=en
S2	0	1	0	01	10	1	1	-	-	32=en	42=dis 42=dis
S3	0	0	1	00	01	0	1	-	1	33=en	43=dis 43=en
S4	0	0	0	00	00	0	0	-	-	34=en	44=dis 44=dis